

Application No.: 09/922,092

Docket No.: JCLA6561-R

AMENDMENTS

In The Claims:

Please amend the claims as follows:

1. (currently amended) A method of bus priority arbitration driven by data used in a bus system that comprises a bus and a plurality of masters connected to the bus, wherein each master can output a request for a grant to use the bus, the method comprising:

sequentially responding to the request of each master according to a predefined orderly rotation, wherein the masters are considered as a group;

stopping a response to the requests of the masters according to the predefined orderly rotation when a data for any one of the masters is ready;

attributing highest priority to the master which the data is ready for the grant to use the bus;

performing the data transfer using the bus; and

resuming a response to the requests of the masters according to the predefined orderly rotation.

2. (original) The method of claim 1, wherein the bus is a peripheral component interconnect (PCI) bus.

3. (original) The method of claim 1, wherein responding to the requests of the masters and attributing the highest priority to the master are performed by a host bridge.

4. (original) The method of claim 3, wherein stopping the response to the requests of the masters is carried out by outputting a stop signal.

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5. (original) The method of claim 1, wherein resuming the response to the requests of the masters according to the predefined orderly rotation is performed from the master which request evaluation has been stopped.

6. (original) The method of claim 1, wherein the steps of resuming the response to the requests of the masters according to the predefined orderly rotation is performed from the master which data transfer has been performed.

7. (currently amended) A peripheral device interconnect structure comprising:

a bus;

a plurality of peripheral devices connected to the bus, the peripheral device are considered as a group, each of the peripheral devices embedding a master;

a host bridge connected to the bus, wherein the host bridge is further operable:

to respond to a plurality of requests from each of the masters according to a predefined orderly rotation;

to receive information indicating that a data transfer for one of the master is ready; and

to stop responding to the requests from each of the masters according to the predefined orderly rotation when receiving information indicating that a data for any one of the peripheral devices is ready in order to attribute the highest priority to said any one of the peripheral devices for granting use of the bus.

8. (original) The structure of claim 7, wherein the host bridge is connected to a data storage device from which the host bridge receives information indicating that a data transfer is ready.